CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of operating a pixel of an image sensor comprising:

accumulating charge in a photosensor;

transferring said charge from said photosensor to a storage node; and

selectively supplying operating power to said pixel to produce an output signal on an output line based on the charge at said storage node.

2. A method of claim 1 further comprising reading out the charge residing on said output line.

3. The method of claim 1, wherein prior to accumulating charge in the photosensor, the photosensor is charged with non-image electrons.

4. The method of claim 3 further comprising removing said non-image electrons from the photosensor leaving some non-image electrons trapped at said photosensor.

5. The method of claim 1, wherein said charge is transferred by turning on a transfer transistor and prior to said accumulation said transfer transistor is turned off.

6. The method of claim 1 further comprising resetting the storage node to a predetermined charge level prior to transferring said charge.

7. The method of claim 1 further comprising transferring overflow charge away from said photosensor during accumulating charge in the photosensor through an anti-blooming transistor.

8. A method of reading charge from pixels of an image sensor comprising:

providing an operating voltage across a source follower transistor;

setting a floating diffusion node to a high reset voltage that exceeds a threshold turn-on voltage of the source follower transistor;

turning on a transfer transistor to transfer a charge to the floating diffusion node changing it to a signal voltage; and

reading a signal provided by the source follower transistor in response to the signal voltage.

9. The method of claim 8 further comprising setting the floating diffusion node to a low reset voltage to turn off the source follower transistor.

10. The method of claim 8, in which the row driver signal is a high signal, the high reset voltage is obtained from the high row driver signal.

11. The method of claim 8 further comprising setting the floating diffusion node to a low reset voltage wherein said low reset voltage is above ground.

12. The method of claim 8, wherein said row driver signal is controlled by a global control signal.

13. The method of claim 8, wherein said transfer transistor is controlled by a row specific control signal.

14. The method of claim 8 further comprising turning on an anti-blooming transistor to transfer overflow charge from a photosensor.

15. A method of resetting a floating diffusion node comprising:

applying a row driver signal to a channel terminal of a reset transistor, the row driver signal having high and low levels; and

selectively applying a reset signal to a gate of said reset transistor to reset the floating diffusion node to one of the high and low levels.

16. The method of claim 15, wherein said channel terminal is a source terminal of said reset transistor.

17. A method of operating a pixel comprising:

setting a storage node to a high reset voltage sufficient to turn on a source follower transistor;

accumulating charge in a photosensor;

turning on a transfer transistor; and

transferring said charge from said photosensor to the storage node through said transfer transistor.

18. The method of claim 17 further comprising transferring overflow charge away from said photosensor during said accumulation through an anti-blooming transistor.

19. A method of operating a pixel comprising:

providing a low signal to a channel terminal of a reset transistor that resets a floating diffusion node;

turning on the reset transistor and a transfer transistor connected between the floating diffusion node and a photosensor;

providing a high signal to the channel terminal of the reset transistor;

turning off the transfer transistor;

providing a low signal to the channel terminal of the reset transistor; and

turning off the reset transistor.

20. The method of claim 19 further comprising charging the photosensor with non-image electrons while the row driver signal is low and the reset transistor and transfer transistor turned on; and

resetting said photosensor by turning off the transfer transistor while providing the high row driver signal, thereby removing a portion of said non-image electrons from said photosensor but leaving some non-image electrons in said photosensor.

21. A method of operating a pixel comprising:

providing a high signal to reset a storage node;

sampling a reset output voltage provided by the resetting of said storage node;

transferring accumulated charge to said storage node; and

sampling a signal output voltage based on said transferring.

22. The method of claim 21 further comprising:

providing a low signal to the channel terminals after sampling the signal output voltage; and

turning the reset transistor on and then off.

23. The method of claim 21 further comprising providing a high signal to a first channel terminal of an anti-blooming transistor and a low signal to a gate terminal of said anti-blooming transistor, the anti-blooming

transistor having a second channel terminal connected to the photosensor thereby permitting flow of charge away from the photosensor.

24. A method of reading a pixel output signal comprising:

providing a row driver signal to said pixel to provide an operating voltage to output an output signal based on voltage on a storage node;

resetting a storage node to a predetermined reset voltage;

reading out the output signal produced by said predetermined reset voltage;

transferring photo-generated charge to said storage node to change said charge at said storage node to a signal voltage; and

reading out the output signal based on the signal voltage.

25. The method of claim 24 further comprising resetting said floating diffusion node to voltage above ground but below a voltage sufficient to turn on the source follower transistor.

26. A method of operating a pixel comprising:

applying a first operating voltage to said pixel which is above a ground potential and below a second operating voltage;

using said first operating voltage to store non-image electrons in a photosensor;

increasing said operating voltage from said first operating voltage to said second operating voltage to drive said non-image electrons from said photosensor; and

using said photosensor to generate electrons from an acquired image.

27. The method of claim 26, wherein said first and second operating voltage is provided by a row driver.

28. A method of operating a pixel comprising:

setting an operating voltage to a second operating voltage from a first operating voltage, said first operating voltage being above ground;

resetting a storage node using said second operating voltage;

transferring charge from a photosensor to a storage node;

setting an operating voltage to said first operating voltage from said second operating voltage after said charge transfer; and

resetting said storage node using said first operating voltage.

29. The method of claim 28 further comprising sampling an output signal produced by charge on said storage node after said storage node is reset using the second operating voltage; and

sampling an output signal produced by charge on said storage node after charge is transferred to said storage node from said photosensor.

30. A method of operating a pixel comprising:

providing an operating voltage across a reset transistor and a source follower transistor, the operating voltage having a high level and a low level;

turning the reset transistor on and off to reset a storage node to the high or low level of the operating voltage; and

turning a transfer transistor on and off to allow charge flow between a photosensor and the storage node, the source follower transistor providing an output signal for the pixel based on the storage node's voltage.

31. A method of operating an array of pixels that includes rows, the method comprising:

providing a row driver signal to a channel terminal of a reset transistor in each pixel in a row of the array and to a channel terminal of a source follower transistor in each pixel in the row; and

turning the reset transistor on and off to reset a storage node in each pixel in accordance with the row driver signal; the storage node receiving charge from a photosensor in the pixel, the source follower transistor providing an output signal for the pixel based on the storage node's voltage.

32. A pixel circuit for use in an imaging device, said pixel circuit comprising:

a photosensor for generating charge during an integration period;

a storage node for receiving said generated charge from said photosensor; and

a readout circuit for reading out stored charge from said storage node, said readout circuit selectively receiving operating power and in response to the selective receipt of operating power at a predetermined level provides an output signal based on the charge accumulated at the storage node.

33. The circuit of claim 32 further comprising a transfer transistor connected to said photosensor to transfer charge from said photosensor to said storage node.

34. The circuit of claim 33, wherein said readout circuit comprises a source-follower transistor having a gate for receiving charge from the storage node, a first source/drain terminal for selectively receiving said operating power, and a second source/drain terminal coupled to a column line.

35. The circuit of claim 34, wherein a turn off voltage for said source follower transistor is above a ground potential.

36. The circuit of claim 32, wherein said readout circuit further comprises a reset transistor connected to said storage node for resetting the voltage on the storage node.

37. The circuit of claim 32, wherein said storage node is at a first voltage prior to receiving charge from the transfer transistor.

38. The circuit of claim 32, wherein said pixel is a three transistor pixel.

39. The circuit of claim 32, wherein said pixel is a CMOS pixel.

40. The circuit of claim 32 further comprising an anti-blooming transistor connected to said photosensor for providing an overflow path for electrons during said integration period.

41. The circuit of claim 40, wherein said pixel is a four transistor pixel.

42. A pixel circuit for use in an imaging device, said pixel circuit comprising:

a photosensor for generating charge during an integration period;

a transfer transistor connected to said photosensor to transfer charge from said photosensor;

a storage node for receiving charge transferred by the transfer transistor;

a reset transistor connected to said storage node for resetting the voltage on the storage node;

a source-follower transistor connected to said reset transistor for receiving charge from the floating diffusion node; and

operating power circuitry connected to said source follower transistor for providing operating power to said source follower transistor for outputting an output signal based on the charge accumulated at the storage node on an output line.

43. The circuit of claim 42 further comprising an anti-blooming transistor connected to said photosensor for providing an overflow path for electrons during said integration period.

44. The circuit of claim 42, wherein said pixel is a CMOS pixel.

45. A pixel circuit for an imaging device comprising:

a photosensor;

a storage node;

transfer circuitry that allows flow of charge between the photosensor and storage node;

a source follower transistor that provides an output signal based on voltage of the storage node;

a reset transistor that when turned on resets the storage node voltage; and

operating voltage circuitry that provides an operating voltage across the source follower transistor and the reset transistor, the operating voltage having a high level and a low level.

46. The pixel circuit of claim 45 in which the transfer circuitry includes a transfer transistor that allows flow of charge when turned on.

47. An integrated circuit comprising:

a plurality of pixels, each pixel comprising:

a photosensor for generating charge during an integration period;

a storage node for receiving said generated charge from said photosensor; and

a readout circuit for reading out stored charge from said storage node, said readout circuit selectively receiving operating power and in response to the selective receipt of operating power at a predetermined level provides an output signal based on the charge accumulated at the storage node.

48. The integrated circuit of claim 47 in which each pixel further comprises a transfer transistor connected to said photosensor to transfer charge from said photosensor to said storage node.

49. The integrated circuit of claim 47, wherein said readout circuit further comprises a reset transistor connected to the storage node for resetting the voltage on the storage node.

50. The integrated circuit of claim 47, wherein said readout circuit further comprises a source-follower transistor having a gate for receiving charge from the storage node a first source/drain terminal for selectively receiving said operating power, and a second source/drain terminal coupled to a column line.

51. The integrated circuit of claim 50, wherein a turn off voltage for said source follower transistor is above ground.

52. The integrated circuit of claim 47 in which the pixels are in rows, the array further comprising a row driver coupled to selectively provide said operating power to each row of pixels.

53. The integrated circuit of claim 47 further comprising an anti-blooming transistor connected to said photosensor for providing an overflow path for electrons.

54. An imaging system comprising:

a processor; and

an imaging device comprising an array of pixels coupled to said processor, each pixel including:

a photosensor for generating charge during an integration period,

a storage node for receiving said generated charge from said photosensor, and

a readout circuit for reading out stored charge from said storage node, said readout circuit selectively receiving operating power and in response to the selective receipt of operating power at a predetermined level provides an output signal based on the charge accumulated at the storage node.

55. The system of claim 54 in which each pixel further comprises a transfer transistor connected to said photosensor to transfer charge from said photosensor to said storage node.

56. The system of claim 54, wherein said readout circuit further comprises a source-follower transistor having a gate for receiving charge from a storage node, a first source/drain terminal for selectively receiving said operating power, and a second source/drain terminal coupled to a column line; and

a row driver coupled to said source-follower transistor for providing said operating power to said pixel.

57. The system of claim 56, wherein said row driver is controlled by a global control signal.

58. The system of claim 54 further comprising an anti-blooming transistor connected to said photodiode for providing an overflow path for electrons.